Practitioner's Docket No.: CAT-12945

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of (1st Inventor): Sorin S. Georgescu
Assignee: Catalyst Semiconductor, Inc.
Serial No.: 10/600,125-~~5592~~ Group No.: 2824
Filed: 6/20/2003 Examiner: Toan K. Le
For: "Non-Volatile Memory Integrated Circuit"

Date: May 9, 2005

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

Sir:

In response to the outstanding Office Action dated March 9, 2005, in which the Examiner imposed a restriction requirement to election of invention for the above-referenced application, Applicant elects to prosecute the invention as in Group 1, Claims 1-21 and 38-52 drawn to a layer structure of a memory device on a substrate, without traverse.

Applicant reserves the right to file divisional applications on the non-elected claims.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

5/9/05 Carrie Reddick
Date Signature: Carrie Reddick